IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor device comprising:

a p-type silicon semiconductor region;

an n-type diffusion region formed in a surface region of the silicon semiconductor region;

an Ni silicide film formed in a surface region of the n-type diffusion region; and

a p-type impurity diffusion layer formed to extend from a surface of the Ni silicide film in a depth direction,

wherein the p-type impurity diffusion layer has an impurity profile in which a peak concentration of not lower than 1E20 cm^{-3} is provided in a preset depth position of the Ni silicide film and a concentration in an interface between the Ni silicide film and the n-type diffusion region and a concentration in a position deeper than the interface are not higher than 5E19 cm^{-3}, and the impurity profile has a peak concentration in the Ni silicide film.

2. (Original) A semiconductor device according to claim 1, wherein the p-type impurity is one of B and F.

3. (Currently Amended) A semiconductor device according to claim 1, wherein the ~~p-type~~ impurity profile has a peak concentration in a position at a depth of 30 nm from the surface of the Ni silicide film.

4. (Original) A semiconductor device according to claim 1, wherein the n-type impurity diffusion region is source or drain region of a MOS transistor.

5. (Original) A semiconductor device according to claim 1, further comprising a contact liner film which is formed on at least the n-type diffusion region and in which opening portion to expose part of the surface of the n-type diffusion region is formed, and an electrode formed in contact with the surface of the n-type diffusion region via the opening portion of the contact liner film.

6. (Currently Amended) A semiconductor device comprising:

a p-type silicon semiconductor region;

a pair of n-type diffusion regions separately formed in a surface region of the silicon semiconductor region;

a gate electrode containing silicon and formed above part of the silicon semiconductor region which lies between the pair of n-type diffusion regions with a gate insulating film disposed therebetween;

a plurality of Ni silicide films formed in surface regions of the pair of n-type diffusion regions and an upper surface region of the gate electrode; and

a pair of p-type impurity diffusion layers formed to extend from surfaces of the Ni silicide films formed in the surface regions of the pair of n-type diffusion regions in a depth direction, each of the p-type impurity diffusion layers has an impurity profile in which a peak concentration of not lower than 1E20 cm-3 is provided in a preset depth position of the Ni silicide film and a concentration in an interface between the Ni silicide film and the n-type diffusion region and a concentration in a position deeper than the interface are not higher than 5E19 cm^{-3}, and the impurity profile has a peak concentration in the Ni silicide film.

7. (Original) A semiconductor device according to claim 6, wherein the p-type impurity is one of B and F.

8. (Currently Amended) A semiconductor device according to claim 6, wherein the ~~p-type~~ impurity profile has a peak concentration in a position at a depth of 30 nm from the surface of the Ni silicide film.

9. (Original) A semiconductor device according to claim 6, wherein the pair of n-type impurity diffusion regions is source and drain regions of a MOS transistor.

10. (Original) A semiconductor device according to claim 6, further comprising a contact liner film which is formed on at least the pair of n-type diffusion regions and in which a pair of opening portions to expose part of the surfaces of the n-type diffusion regions are formed, and a pair of electrodes formed in contact with the surfaces of the pair of n-type diffusion regions via the pair of opening portions of the contact liner film.

11. (Currently Amended) A manufacturing method of a semiconductor device comprising:

doping n-type impurity ions into a selected portion of a surface region of a p-type silicon semiconductor region;

doping p-type impurity ions into the entire surface region of the silicon semiconductor region;

activating the n-type and p-type impurity ions to form an n-type diffusion region in the surface region of the silicon semiconductor region and form a p-type impurity diffusion layer in a depth direction of the silicon semiconductor region; and

performing heat treatment to form an Ni silicide film in the surface region of the n-type diffusion region after depositing Ni on the surface of the n-type diffusion region,

wherein the p-type impurity diffusion layer is formed after formation of the Ni silicide film to have an impurity profile in which a peak concentration of not lower than 1E20 cm^{-3} is provided in a preset depth position of the Ni silicide film and a concentration in an interface between the Ni silicide film and the n-type diffusion region and a concentration in a position deeper than the interface are not higher than 5E19 cm^{-3}, and the p-type ions are doped to provide a peak concentration in the Ni silicide film.

12. (Original) A manufacturing method of the semiconductor device according to claim 11, wherein one of B and BF_2 ions is doped as the p-type impurity.

13. (Original) A manufacturing method of the semiconductor device according to claim 11, wherein the p-type impurity ions are doped to provide a peak concentration in a position at a depth of 30 nm from the surface of the Ni silicide film.

14. (Original) A manufacturing method of the semiconductor device according to claim 11, further comprising:

forming a contact liner film on the entire surface after forming the Ni silicide film;

forming an inter-level insulating film on the entire surface;

forming opening portion which reaches the surface of the n-type diffusion region in the inter-level insulating film and contact liner film; and

forming an electrode in contact with the surface of the n-type diffusion region in the opening portion.

15. (Currently Amended) A manufacturing method of a semiconductor device comprising:

doping p-type impurity ions into an entire surface region of a p-type silicon semiconductor region;

doping n-type impurity ions into a selected position of the surface region of the silicon semiconductor region;

activating the p-type and n-type impurity ions to form a p-type impurity diffusion layer in a depth direction of the silicon semiconductor region and form an n-type diffusion region on the surface portion of the silicon semiconductor region; and

performing heat treatment to form an Ni silicide film on the surface region of the n-type diffusion region after depositing Ni on the surface of the n-type diffusion region,

wherein the p-type impurity diffusion layer is formed after formation of the Ni silicide film to have an impurity profile in which a peak concentration of not lower than 1E20 cm^{-3} is provided in a preset depth position of the Ni silicide film and a concentration in an interface between the Ni silicide film and the n-type diffusion region and a concentration in a position deeper than the interface are not higher than 5E19 cm^{-3}, and the p-type ions are doped to provide a peak concentration in the Ni silicide film.

16. (Original) A manufacturing method of the semiconductor device according to claim 15, wherein one of B and BF_2 ions is doped as the p-type impurity.

17. (Original) A manufacturing method of the semiconductor device according to claim 15, wherein the p-type impurity ions are doped to provide a peak concentration in a position at a depth of 30 nm from the surface of the Ni silicide film.

18. (Original) A manufacturing method of the semiconductor device according to claim 15, further comprising:

forming a contact liner film on the entire surface on the entire surface after forming the Ni silicide film;

forming an inter-level insulating film on the entire surface;

forming opening portion which reaches the surface of the n-type diffusion region in the inter-level insulating film and contact liner film; and

forming an electrode in contact with the surface of the n-type diffusion region in the opening portion.

19. (Currently Amended) A manufacturing method of a semiconductor device comprising:

doping n-type impurity ions into a selected position of a surface region of a p-type silicon semiconductor region;

activating the n-type impurity ions to form n-type diffusion region on the surface portion of the silicon semiconductor region;

doping p-type impurity ions into an entire surface portion of the silicon semiconductor region to form the surface portion of the silicon semiconductor region in an amorphous form;

activating the p-type impurity ions to form p-type diffusion region in a depth direction of the silicon semiconductor region; and

performing heat treatment to form an Ni silicide film on the surface region of the n-type diffusion region after depositing Ni on the surface of the n-type diffusion region,

wherein the p-type impurity diffusion layer is formed after formation of the Ni silicide film to have an impurity profile in which a peak concentration of not lower than 1E20 cm^{-3} is provided in a preset depth position of the Ni silicide film and a concentration in an interface between the Ni silicide film and the n-type diffusion region and a concentration in a position deeper than the interface are not higher than 5E19 cm^{-3}, and the p-type ions are doped to provide a peak concentration in the Ni silicide film.

20. (Original) A manufacturing method of the semiconductor device according to claim 19, wherein one of B and BF_2 ions is doped as the p-type impurity.

21. (Original) A manufacturing method of the semiconductor device according to claim 19, wherein the p-type impurity ions are doped to provide a peak concentration in a position at a depth of 30 nm from the surface of the Ni silicide film.

22. (Original) A manufacturing method of the semiconductor device according to claim 19, further comprising:

forming a contact liner film on the entire surface after forming the Ni silicide film;

forming an inter-level insulating film on the entire surface;

forming an opening portion which reaches the surface of the n-type diffusion region in the inter-level insulating film and the contact liner film; and

forming an electrode in contact with the surface of the n-type diffusion region in the opening portion.